Claims

1. A method of making pairs of floating gate memory transistors with symmetric floating gates comprising,

making a floating poly member on a semiconductor substrate having an oxide covering,

implanting self-aligned highly doped regions in the substrate on opposite lateral sides of the floating poly member,

surrounding said floating poly member with planarized insulative material,

etching away said floating poly member from the insulative material except for two poly remnants adjacent to the insulative material and laterally spaced apart,

insulating the two laterally spaced apart poly remnants,

disposing a control gate over the insulated laterally spaced poly remnants and

electrically connecting the substrate, the control gate, the floating gates and the highly doped regions to make two independent memory transistors.

2. The method of claim 1 wherein said placing of highly doped regions in the substrate on opposite lateral sides of the floating poly member with insulative material is further defined by ion implantation.

3. The method of claim 1 further defined by planarizing the surrounded poly member.

4. The method of claim 3 wherein the planarizing step is carried out by chemical-mechanical polishing.

5. The method of claim 1 wherein said floating poly member is covered with nitride prior to said implanting step.

6. The method of claim 1 wherein said poly remnants are covered with nitride.

7. The method of claim 6 further defined by removing said nitride covering before the step of insulating the two laterally spaced apart poly remnants.

8. The method of claim 1 further defined by electrically connecting the two memory transistors to two-phased bit lines for alternating access to the two transistors.

9. A method of making pairs of floating gate memory transistors with floating gates smaller than a minimum feature size of a manufacturing process comprising,

making a minimum feature size floating poly member on a semiconductor substrate having an oxide covering,

placing highly doped regions in the substrate on opposite lateral sides of the minimum feature size floating poly member,

surrounding said minimum feature size floating poly member with insulative material,

etching away said minimum feature size floating poly member from the insulative material except for two poly remnants adjacent to the insulative material and laterally spaced apart by less than said minimum feature size floating poly member with a corresponding feature size substantially smaller than the minimum feature size floating poly member,

insulating the two laterally spaced apart poly remnants,

disposing a control gate over the insulated laterally spaced poly remnants and

electrically connecting the substrate, the control gate, the floating gates and the highly doped regions to make two independent memory transistors.

10. The method of claim 9 wherein said placing of highly doped regions in the substrate on opposite lateral sides of the minimum feature size floating poly member with insulative material is by ion implantation.

11. The method of claim 9 wherein the making of a minimum feature size floating poly member on a semiconductor substrate is done by defining the minimum feature size with a semiconductor manufacturing tool.

12. The method of claim 11 where said tool comprises a photolithographic mask.

13. The method of claim 11 wherein said tool comprises a beam.

14. The method of claim 9 further defined by planarizing the surrounded minimum feature size poly member.

15. The method of claim 14 wherein the planarizing step is carried out by chemical-mechanical polishing.

16. The method of claim 9 wherein said minimum feature size floating poly member is covered with nitride.

17. The method of claim 9 wherein said poly remnants are covered with nitride.

18. The method of claim 17 further defined by removing said nitride covering before the step of insulating the two laterally spaced apart poly remnants.

19. The method of claim 9 further defined by electrically connecting the two memory transistors to two-phased bit lines for alternating access to the two transistors.

20. A pair of non-volatile memory transistors comprising,

a pair of floating gates disposed over an insulated substrate, the floating gates spaced apart by a distance less than the minimum feature size of a chip manufacturing process,

a pair of highly doped regions laterally outward of the pair of floating gates in band-to-band tunneling relation with the pair of floating gates, and

a single conductive control layer spaced in insulated relation over the pair of floating gates, the control layer electrically communicating with the substrate, the control gate, the floating gates and the highly doped regions to make two independent memory transistors.